

Application No.: 10/656,006

Docket No.: JCLA11225

**REMARKS****Present Status of the Application**

The Office Action objected claims 9-15 as having minor errors. Claims 8-15 are pending. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Man et al. (US Patent Application No. 2003/0101391) in view of Day et al. (US-5,663,966). In addition, Claims 9-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

After entry of the foregoing amendments and traversing of rejections, claims 8-15 remain pending in the present application, and reconsideration of those claims is respectfully requested.

**Discussion of Objections**

Claims 9-15 are objected to as having a minor error, and reconsideration is respectfully requested. Claims 9-15 are allowable once the minor corrections are done.

In response thereto, Claim 9-15 has been amended to correct the minor error.

In view of the aforementioned, Applicants respectfully assert that the objections are no longer proper.

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**Discussion of the claim rejection under 35 USC 103**

*The Office Action rejected claim 8 under 35 U.S.C. 103(a) as being unpatentable over Man et al. (US Patent Application No. 2003/0101391, hereinafter "Man") in view of Day et al. (US-5,663,966, hereinafter "Day").*

Man discloses a "System for testing multiple devices on a single system and method". Under this infrastructure, one can by means of a single HOST SYSTEM, a "Tester Port" 122, a "Bridge Chip" 124, and using different device interconnecting interfaces to test a plurality of different devices, including DVD. It is primarily focused on the "Tester Application" 107 for a single HOST SYSTEM, which is coupled to interfaces for switching between testing of different devices. The aforementioned is a conventional testing infrastructure, which is clearly different from the Applicants'.

The objective of the present invention is to primarily propose a testing board for DVD ROM chipset; and this testing board has a phase-shift RF signal generating circuit. As the testing system provides a digital input signal which varies with a frequency for conducting testing to the DVD ROM chipset, it is able to utilize phase-shift RF signal generating circuit for producing the required phase-shift RF signal during the testing of the analog circuit block of DVD ROM chipset. This not only can be used for testing the digital circuit of the DVD ROM chipset, but can also be used to test the analog circuit block of DVD ROM chipset. The aforementioned is not taught, suggested, or disclosed in Man.

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Furthermore, the Examiner has stated that although Man did not teach the "phase-shift RF signal generating circuit" in the present invention. However, Day in Col. 8, lines 8-45 has already disclosed the "first phase-shift RF signal, a second phase-shift RF signal, a third phase-shift RF signal, and a fourth phase-shift RF signal for testing the DVD ROM chipset, wherein the first phase-shift RF signal and the second phase-shift RF signal are in phase, and are differed by a phase shift from the third phase-shift RF signal and the fourth phase-shift RF signal" in claim 8 of the Applicants'. Therefore, the premise of a person skilled in the art that can use Man in view of Day to obtain the features of the Applicants' claim 8 is an incorrect determination and is unreasonable to accept.

Day primarily discloses "System and method for minimizing simultaneous switching during scan-based testing". In Col. 8, lines 8-45 in Day :

Referring now to FIG. 11, the generation of multiple scan clock groups is shown. Where one or more chips under test are logically divided into two clusters, two scan clock groups are used. A first scan clock group is used to clock the scan shifts in the first cluster, and a second scan clock group is used to clock the scan shifts in a second cluster.

Clock generator 220 generates a C1 clock signal on line 132 as was described for clock generator 160 of FIG. 5. However, rather than generating one A clock signal and one C2/B clock signal as shown on lines 136 and 140 respectively of FIG. 5, two A clock and C2/B clock signals are generated by the clock generator 220 of FIG. 11. The A1 clock signal on line 222 and the A2 clock signal on line 224 each clock the scan chains in different clusters.

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For instance, the scan chains of cluster 212 of FIG. 10 will have their L1 latches in each SRL clocked by the A1 clock signal on line 222, and the scan chains of cluster 214 of FIG. 10 will have their L1 latches in each SRL clocked by the A2 clock signal on line 224.

The C2/B1 clock signal on line 226 is the B1 clock signal from line 228 during scan shift operations. The C2 clock signal on line 230 will be inhibited by the clock generator 220 during scan shift operations, thereby allowing the B1 clock signal on line 228 to pass through OR gate 232 to become the C2/B1 clock signal on line 226. Likewise, the C2/B2 clock signal on line 232 is the B2 clock signal from line 234 during scan shift operations, because the B2 clock signal on line 234 will pass through OR gate 236 to become the C2/B2 clock signal on line 232. The C2/B1 clock signal on line 226 and the C2/B2 clock signal on line 232 also each clock the scan chains in different clusters. For instance, the scan chains of cluster 212 of FIG. 10 will have their L2 latches in each SRL clocked by the C2/B1 clock signal on line 226, and the scan chains of cluster 214 of FIG. 10 will have their L2 latches in each SRL clocked by the C2/B2 clock signal on line 232. Note that it is not necessary to pair the A1 and B1 signals, since the A1 and B2 signals could actually be "paired", as long as the switching is not occurring simultaneously.

FIG. 12 is a waveform diagram showing the relationship of the scan clock groups. Referring now to FIGS. 11 and 12, the A1 clock signal on line 222 and the C2/B1 clock signal on line 226 jointly make up a first scan clock group which clocks a series of scan shifts A1/B1. The

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A1 clock signal and the C2/B1 clock signal operate analogously to the A clock signal and the C2/B clock signal of FIG. 7. The scan clock group including the A1 clock signal and the C2/B1 clock signal clock a first cluster, such as cluster 212 of FIG. 10.

The aforementioned section is primarily used for providing the clock signals C1, C2, B1, B2, A1, and A2 for scan-based testing, and the C2/B2 or the C1/B2 are mutually inhibiting. The clock signals C1, C2, B1, B2, A1, and A2 generated from the clock generator 220 for scan-based testing are all digital clock signals. The aforementioned section is completely different in comparison to the Applicants' having a phase-shift analog-typed first through fourth phase-shift RF signal. Therefore, it is inconceivable how someone who is skilled in the art is able to obtain the features as set forth in claim 8 by using Man in view of Day? Therefore, as can be deduced, claim 8 patentably distinguish over Man in view of Day. Thus, claim 8 should be allowed. In addition, dependent claims 9-15 should also be allowed since if claim 8 is allowed.

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**CONCLUSION**

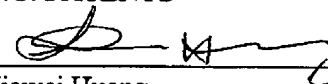
For at least the foregoing reasons, it is believed that all the pending claims 8-15 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,  
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